

UNDER 35 USC 371

5397432

SERIAL
NUMBER
(Series
of 1987)

743353

PATENT DATE

AUG 11 1995

PATENT
NUMBER



NUMBER 43,393	FILING DATE 08/21/91	CLASS 156	SUBCLASS 665 665	GROUP/ART UNIT 1109	EXAMINER Goudreau
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ON: CHI KONNO, MIE, JAPAN; KEISUKE SHINAGAWA, KANAGAWA, JAPAN;
YOSHIYUKI ISHIDA, KANAGAWA, JAPAN; TAKAHIRO ITO, KANAGAWA, JAPAN;
TAKESHI KONDO, KANAGAWA, JAPAN; FUKASHI HARADA, MIE, JAPAN; SHUZO
UJIYAMA, TOKYO, JAPAN

36Kt

CONTINUING DATA*****
VERIFIED

9-92

INTERNATIONAL APPLICATIONS*****

FILED	PCT	PCT/JF91/00861	06/26/91
JAPAN		2-171791	06/27/90

claimed ditions met	<input checked="" type="checkbox"/> yes <input type="checkbox"/> no	<input type="checkbox"/> yes <input checked="" type="checkbox"/> no	AS FILED	STATE OR COUNTRY	SHEETS DRWGS.	TOTAL CLAIMS	INDEP. CLAIMS	FILING FEE RECEIVED	ATTORNEY'S DOCKET NO.
known	Examiner's initials		→	JFX	7	22	4	\$560.00	911333

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FOR PRODUCING SEMICONDUCTOR INTEGRATED CIRCUITS AND APPARATUS
IN SUCH METHOD

U.S. DEPT. of COMM. Pat. & TM Office - PTO-436L (Rev. 10-78)

ITS OF APPLICATION
AND SEPARATELY

NOTICE OF ALLOWANCE MAILED		PREPARED FOR ISSUE 9-28-94		CLAIMS ALLOWED	
9-16-94		George Goudreau Assistant Examiner	Richards Docket Clerk	Total Claims 19	Print Claim 1
ISSUE FEE		R. BRUCE BRENNAN Supervisory Patent Examiner Art Unit 1109 Primary Examiner		DRAWING	
Amount Due 170.00	Date Paid 12-9-94			Sheets Drwg. 6	Figs. Drwg. 13
Label Area	ISSUE CLASSIFICATION		ISSUE BATCH NUMBER		
	Class 156	Subclass 665	ES1		
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